REMARKS/ARGUMENTS

1. Rejection of claims 1-5 under 35 U.S.C. 103(a) as being unpatentable over Matsumoto et al. (US 5,365,284) in view of Kim (US 5,808,596) and Uehara et al. (US 6,329,980): Response:

Claim 1:

Claim 1 has been amended to overcome this rejection. Specifically, the limitation "the timing signals are transmitted to different logic circuits with the same function by a plurality of transmitting lines, and differences between a product of an equivalent resistance value and an equivalent capacitance value of each transmitting line are less than 1000 μs" has been added to claim 1. This limitation was originally recited in claim 2, and no new matter is introduced by this amendment. Acceptance of this amendment is therefore requested.

Matsumoto discloses an LCD panel, which uses two data line drivers to control the display cells of the LCD panel, however, Matsumoto fails to explicitly or implicitly teach determining a location in the panel for forming the timing control circuit so as to make differences among delay time intervals of the timing signals transmitted to different logic circuits with the same function less than 1000 μs, and forming the timing control circuit accordingly.

In view of the insufficiency of Matsumoto's disclosure, the Examiner cited US 5,808,596 which teaches that two data line drivers can receive synchronized timing signals. Nevertheless, Kim teaches using an arithmetic operator 500 and a delay circuit 600 to synchronize the timing signals delivered to different data line drivers. As illustrated in Kim's col. 3, lines 25-65, col. 4, lines 32-34, Fig. 1, both of the arithmetic operator 500 and the delay circuit 600 receive an input pixel data (a). The arithmetic operator 500, electrically connected to a second data driver 310, is responsible for averaging adjacent input pixel data values and supplying the average adjacent input pixel data values (c) to the second data driver 310; The

delay circuit 600, electrically connected to the arithmetic operator 500 and a first data driver 300, **imparts a sufficient time delay to the input pixel data (a) to synchronize the average adjacent pixel data (c)** which is applied to the second data driver with the time delayed input pixel data (b) applied to the first data driver 300. Evidently, Kim **uses the delay circuit 600, which includes flip-flops in a cascaded arrangement, to delay the input pixel data (b) applied to the first data driver 300** such that the input pixel data (b) and the input pixel data (c) are synchronized.

On the contrary, the method according to the amended claim 1 synchronizes the timing signals delivered to different logic circuits by **determining the location in the panel for forming the timing control circuit** so as to make differences among delay time intervals of the timing signals transmitted to different logic circuits with the same function less than 1000 μs, and forming the timing control circuit accordingly. Specifically, the physical location of the timing control circuit in the panel makes the timing control signals delivered to different logic circuits synchronized. Also, the timing signals are transmitted to different logic circuits with the same function by a plurality of transmitting lines, and the **determination of the location** of the timing control circuit makes the differences between the product of an equivalent resistance value and an equivalent capacitance value of each transmitting line are less than 1000 μs.

Compared with claim 1, Kim uses the delay circuit 600 including flip-flops to synchronize the timing control signals delivered to different data drivers. According to Kim's disclosure, the different between the product of an equivalent resistance value and an equivalent capacitance value with respect to the transmitting line delivered to the first data driver 300 and the product of an equivalent resistance value and an equivalent capacitance value with respect to the transmitting line delivered to the second data driver 310 would not less than 1000 μs **because Kim's uses the delay circuit 600 to**

synchronize the timing control signals, instead of equalizing the physical condition of the transmitting lines connected to different data drivers.

As a result, claim 1 and Kim implement the synchronization of the timing control signals by different means. In addition, the method according to claim 1, compared with Kim's teaching which uses additional delay circuit, has the advantages of lower cost, higher reliability, and less interference between electronic devices because no additional electronic device for synchronization is added in the panel. Thus, claim 1 should be patentably distinct from Kim's teaching, and reconsideration of claim 1 is respectfully requested.

Claim 2:

Claim 2 has been cancelled.

Claims 3, 5:

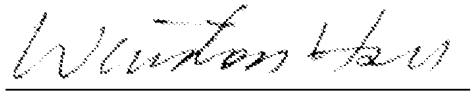
Claims 3 and 5 are dependent on claim 1, and should be allowed if claim 1 is found allowable. Reconsideration of claims 3 and 5 is politely requested.

Claim 4:

Claim 4 teaches the limitation "the timing signal is respectively transmitted to the first data line driving circuit and to the second data line driving circuit by a first transmitting line and a second transmitting line, differences between a product of an equivalent resistance value and an equivalent capacitance value of the first transmitting line and a product of an equivalent resistance value and an equivalent capacitance value of the second transmitting line being less than $1000\,\mu s$". Kim uses the delay circuit 600 to synchronize the timing control signals, and thus Kim's transmitting lines connected to the first data driver 300 and the second data driver 310 fail to fulfill this limitation. Therefore, claim 4 should be patentable, and reconsideration of claim 4 is respectfully requested.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,



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